A Test for Multiple Signaling Frames and B8ZS Mismatch

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1 Introduction

Sage has designed a special Bit-Error-Rate type of test. We will abbreviate this test as SPBERT from here on. SPBERT accomplishes the following 3 goals:

1. Detect multiple signaling frames on a DS0 channel and display the associated signaling bits pattern (the so-called "ABCD" bits).
2. Identify B8ZS mismatch problem and display the "corrupted" all-zero pattern.
3. Perform DS0 56Kbps BER measurement.

This SPBERT is a pure DS0-level DSP-software-based test. It operates like a normal DSP test such as sending-tone and measuring-tone etc. Once a call connection is established, one box (or one port or one channel) can send the special test pattern, while the other box (or another port or another channel) measures the test pattern. If a DS1 or DS0 loopback is available at the other end, a single box can send and measure simultaneously.

Unlike the existing BERT features Sage offers now, this SPBERT does not require any firmware changes on the T1 boards. This SPBERT is a pure software-based DSP test. Therefore, it can be easily intergrated/ported into Sage's existing platforms with T1 interfaces, such as 935, 94x and 950.

This SPBERT uses a smart algorithm to locate the multiple signaling frames from the plain 64Kbps DS0 data stream itself without the need for explicit framing-bit information from the T1 boards. This algorithm allows the detection of multiple signaling frames.

When detecting B8ZS mismatch, a maximum-likelihood algorithm is used. This allows the test to work reliably over an envrironment where there might be excessive bit-errors or the device under test has unpredictable dynamic behavior in bipolar violations.

2 Cause of Multiple Signaling Frames

On a T1 circuit using robbed-bits signaling, the sending-end (data source end) inserts signaling bits onto the LSBs (least-significant-bits) of the 24 DS0 PCM bytes within the signaling frame.

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This signaling frame occurs once every 6 frames (once every $6 \times 0.125 = 0.75$ms). On a specific DS0 channel, the resulting 1333bps signaling bits can either be structured as "AB" pattern in SF (super-frame) format or as "ABCD" pattern in ESF (extended super-frame) format. If this DS0 channel is to be used to carry G.711 encoded audio (voice) signal, these in-band signaling bits will cause minor signal degradation manifested as 1 to 2 dB drop in measured SNR (Signal-to-Noise-Ratio). If this DS0 channel is to be used as a data channel, then the actual usable bandwidth is only $\frac{47}{48} \times 64000 = 62667$bps, instead of the theoretical 64000 bps. Quite often, the DS0 channel is only used as a 56000 bps channel by ignoring all the LSBs.

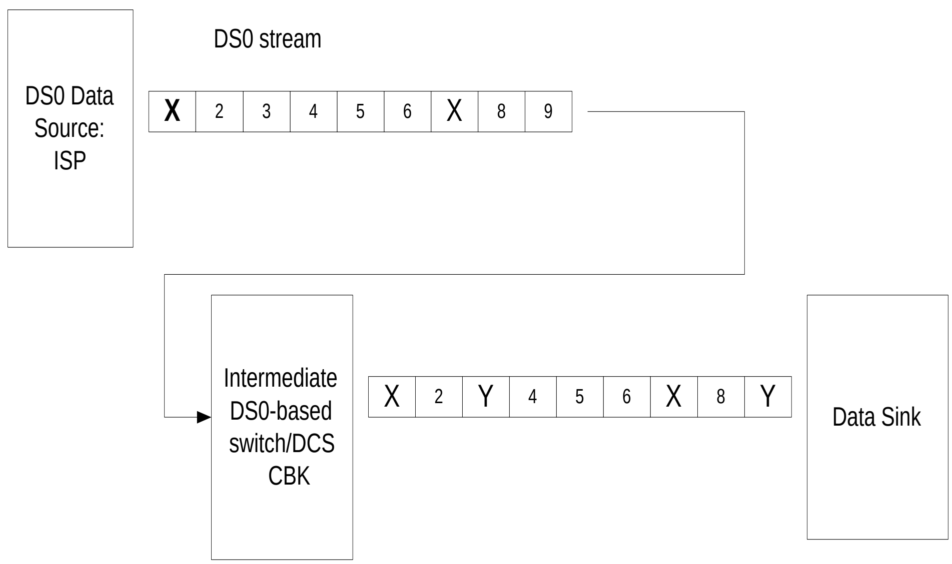

Figure 1: Cause of multiple signaling frames. The data source inserts signaling bits onto the DS0 frames/bytes that are marked as "X". This occurs once every 6 frames. The intermediate switch/DCS/channel bank inserts another sequence of signaling bits onto the DS0 bytes/frames marked as "Y". The data sink, therefore, sees the LSBs being "robbed" more frequent than once every 6 frames.

Certain modem devices, however, detect the exact signaling frame, and can therefore maximize the available bandwidth. For such devices to work correctly, the signaling frame should occur no more frequent than once very 6 frames. But, in certain situations, the signaling frames do occur more frequent than once every 6 frames. Figure 1 shows such scenario.

In reference to Figure 1, the intermediate T1 device (switch, DCS, channel bank or PBX etc) only guarantees bit synchronization, not frame synchronization. This intermediate switch device may insert additional signaling bits onto the frames other than the original signaling frames used by the data source. The data sink, therefore, sees more robbed bits, or more signal degradations or lesser available data bandwidth in this situation. Sage's SPBERT detects, at the data sink side, all signaling bits and display their "ABCD" patterns.

3 B8ZS Mismatch

In a synchronous transmission mode, the transmitted signal waveforms need to have sufficient signal transitions for the receiver to maintain clock synchronization and reduce bit-error-rate. In

T1 transmission, this requirement implies that there must be adequate number of alternating pulses (high enough 1's density with AMI line coding). To maintain high 1's density, yet with no undue restriction on the source data, a B8ZS line coding is commonly used. By B8ZS, an all-zero DS0 PCM byte (8 consecutive binary 0s) are encoded into a special waveform with intentional bipolar violations (against the AMI line coding's premise that each consecutive pulse pair must have alternating polarities). Figure 2 graphically illustrates the B8ZS coding waveform and the cause of B8ZS mismatch problem.

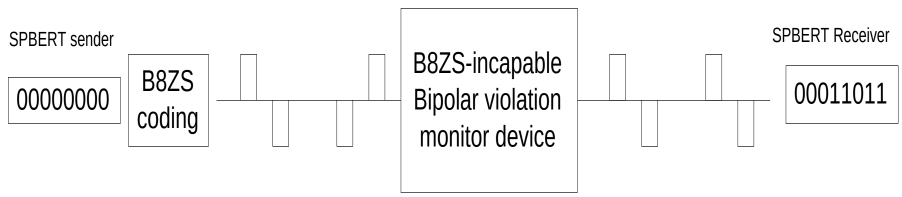

Figure 2: B8ZS mismatch problem. When the sending side (left) needs to send all-zero pattern, and if the device is B8ZS-capable, the T1 driver will generate a special waveform (shown in the middle) to represent this all-zero pattern. Notice that the waveform contains delibrate bipolar violations (the two negative pulses should have opposite polarities according to strict AMI format). If a B8ZS-incapable device is present on the circuit under test, such waveform will be detected as bipolar violations, and the B8ZS waveforms will be incorrectly decoded as "00011011" instead of the original "00000000" pattern. Such is the B8ZS mismatch problem.

As shown in Figure 2, B8ZS mismatch will severely limit the circuit usability in carrying data. Therefore, it needs to be measured and removed. Sage's SPBERT sender will send an all-zero pattern (once every 48 frames), and the SPBERT receiver will locate the exact position of this all-zero byte (through robust synchronization scheme) and decode its pattern. The received "all-zeor" pattern may vary due to either random bit errors or the undeterministic handling of bipolar violations by the circuit under test. Sage's SPBERT will display the most probable (the most-frequently-occurred) pattern. If this pattern is non-zero, it means there is B8ZS mismatch problem. If the pattern is all-zero, then there is no mismatch problem.

4 Operational Details on SPBERT

4.1 User-selectable parameter

When performing the SPBERT test, the user can select the test duration from 1s to 99s. The test duration is counted from the moment the test signal pattern is been detected and synchronized.

The test pattern is fixed, and optimized for signaling frame and B8ZS mismatch detection. The test pattern also contains randomly-distributed near-equal-density of binary 1s and 0s, thereofore, it is also ideal for BER measurement.

4.2 Fault tolerance and error protection

Once SPBERT is started, the test signal pattern should be on the circuit within 20 seconds. If the test signal is not detected within 20 seconds, SPBERT will time out.

For each data buffer SPBERT is processing, the data is checked to see if the valid signal is still there to avoid erroneous readings. If the signal is invalid (signal turned off or circuit gets disconnected), then SPBERT will restart the synchronization process and the measurement will be started all over again until reliable readings are obtained.

4.3 Test results

The following results will be presented by this SPBERT:

```
Number of Signaling Frames: 2
Signaling bits patterns (ABCD bits): 1010, 0111
B8ZS all-zero pattern: 00011101
BER: 1.23E-6
```

In the example shown above, SPBERT detected 2 signaling frames. Ideally, there should only be 1. 2 indicates potential problem. On a clear channel, the number should 0. The maximum number of signaling frames is 6.

The displayed signaling bits patterns provide more details on the signaling frames. The number of patterns displayed will match the number of signaling frames detected. Notice that a specific signaling bits pattern should be interpreted "circularly". For example, the displayed "1010" pattern can be interpreted as "ABCD", or it can be "ABAB", or it can be "BCDA", or it can be "CDAB", or it can "BABA" and etc. And there is no way to tell which signaling frame is primary and which one is secondary. The main purpose here is to show there is additional signaling frame that may cause potential problems.

The received B8ZS-encoded all-zero pattern ("00011101") in this example shows that there is a B8ZS mismatch problem. If the displayed pattern is "00000000", then there is no B8ZS mismatch problem.

The bit-error-rate is a relative ratio (number of errored bits divided by the total number of bits examined). Notice that the examined bits do not include the LSBs, nor does it include the all-zero pattern which occurs once every 48 frames.

4.4 Test signal pattern

The test signal is a periodic bit pattern. The period is 48 bytes (or 6 ms). A complete list of one period of the signal is shown below. The data should be read from left to right, row-by-row.

```
00000000 01010010 01010100 01010110 01011000 01011010
01011100 01011110 01100000 01100010 01100100 01100110
01101000 01101010 01101100 01101110 01110000 01110010
01110100 01110110 01111000 01111010 01111100 01111110
10000001 10000011 10000101 10000111 10001001 10001011
10001101 10001111 10010001 10010011 10010101 10010111
10011001 10011011 10011101 10011111 10100001 10100011
10100101 10100111 10101001 10101011 10101101 10101111
```

The test signal has the following attributes:

1. The first byte is an all-zero byte. It is used to detect the B8ZS mismatch problem.
2. The LSBs of the first 24 bytes are 0s, and the LSBs of the second 24 bytes are all 1s. This pattern is so chosen to facilitate the detection of any form of signaling bit pattern.
3. The pattern has near equal-density of 1s and 0s. This is so chosen to facilitate a “fair” BER measurement.